Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 4. (Canceled).

5. (Currently Amended) A logic verification system comprising:

a storage section for storing an object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase,

an RT level description generated from the behavioral level description,

correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and

compile information ~~including~~ which includes mapping information ~~between~~ which specifies information on a pair of a description fragment of the behavioral level description and a code portion of the object code and which specifies information on a pair of a signal in the behavioral level description and a variable in the object code;

a first logic cone extraction section ~~for extracting~~ configured to extract first logic cones of variables by:

searching a code portion and the variables of the object code corresponding to each fragments of descriptions and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information,

setting initial symbol values in the variables,

performing symbolic simulation from the start to end points of the code portion to produce symbol values when the variable symbolic simulation ends, and

using the symbol values as the first logic cones of the variables;

a second logic cone extraction section ~~for extracting~~ configured to extract second logic cones each for the signals for each fragments of description of RT level description to be compared which are specified by the correspondence information;

a logic cone comparison section ~~for comparing the first logic cones and the second logic cones for each signals for each of the fragments of descriptions~~ configured to select a corresponding logic cone, as a first logic cone, from among the logic cones extracted by the first logic cone extraction section by referencing the compile information, to select a corresponding logic cone, as a second logic cone, from among the logic cones extracted by the second logic cone extraction section by referencing the correspondence information, and to compare the first logic cone and the second logic cone, for each signal and description fragment to be compared in the behavioral level description and the RT level description which are specified by the correspondence information; and

means for determining, based on the comparison of the first logic cones and the second logic cones, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

6. – 11. (Canceled).

12. (Currently Amended) A logic verification method comprising the steps of:

inputting an object code compiled from an behavioral level description written in a programming language, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and compile information ~~including~~ which includes mapping information ~~between~~ which specifies information on a pair of a description fragment of the behavioral level description and a code portion of the object code and which specifies information on a

pair of a signal in the behavioral level description and a variable in the object code, the object code being used for specification verification by simulation on a CPU in a design phase;

searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

setting initial symbol values in the variables;

performing symbolic simulation from the start to end points of the code portion;

determining first logic cones of the variables as symbol values when the variable symbolic simulation ends;

extracting second logic cones each for the signals for each fragments of RT level description to be compared which are specified by the correspondence information;

selecting corresponding logic cones, as first selected logic cones, from among the logic cones determined in the determining step by referencing the compile information;

selecting corresponding logic cones, as second selected logic cones, from among the logic cones extracted in the extracting step by referencing the correspondence information;

comparing the first selected logic cones and the second selected logic cones for each of the signals and for each of the descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information;

determining, based on the comparing step, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits; and

if the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first selected logic cones are logically equivalent to the second selected logic cones.

13. – 16. (Canceled).

17. (Currently Amended) A computer-readable medium embodying a computer program product and comprising code that, when executed, causes a computer to perform logic verification, the program product comprising the steps of:

a) storing an object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and compile information ~~including~~ which includes mapping information ~~between~~ which specifies information on a pair of a description fragment of the behavioral level description and a code portion of the object code and which specifies information on a pair of a signal in the behavioral level description and a variable in the object code;

b) extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language;

c) extracting second logic cones from an RT level description;

d) selecting corresponding logic cones, as first selected logic cones, from among the logic cones determined in the step b) by referencing the compile information;

e) selecting corresponding logic cones, as second selected logic cones, from among the logic cones extracted in the step c) by referencing the correspondence information;

[[d)]] f) comparing the first selected logic cones and the second selected logic cones to verify equivalence between the first and second selected logic cones; and

[[e)]] g) determining, based on the comparison of the first selected logic cones and the second selected logic cones, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable in a manufacturing phase for the logic circuits; and

[[f)]] h) if the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first selected logic cones are logically equivalent to the second selected logic cones,

wherein the step b) comprises the steps of:

b.1) searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

b.2) setting initial symbol values in the variables;

b.3) performing symbolic simulation from the start to end points of the code portion; and

b.4) determining the first logic cones of the variables as symbol values when the variable symbolic simulation ends.

18. – 21. (Canceled).

22. (New) A logic verification system comprising:

a storage section configured to store a behavioral level description written in a programming language,

an RT level description generated from the behavioral level description,

correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and

a compiler section configured to output an object code, which is compiled from the behavioral level description and is executable by a CPU, and compile information including mapping information which specifies information on a pair of a description fragment of the behavioral level description and a code portion of the object code and which specifies information on a pair of a signal in the behavioral level description and a variable in the object code;

a first logic cone extraction section configured to extract first logic cones of variables by:

searching a code portion and the variables of the object code corresponding to each fragments of descriptions and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information,

setting initial symbol values in the variables,

performing symbolic simulation from the start to end points of the code portion to produce symbol values when the variable symbolic simulation ends, and

using the symbol values as the first logic cones of the variables;

a second logic cone extraction section configured to extract second logic cones each for the signals for each fragments of description of RT level description to be compared which are specified by the correspondence information;

a logic cone comparison section configured to select a corresponding logic cone, as a first logic cone, from among the logic cones extracted by the first logic cone extraction section by referencing the compile information, to select a corresponding logic cone, as a second logic cone, from among the logic cones extracted by the second logic cone extraction section by referencing the correspondence information, and to compare the first logic cone and the second logic cone, for each signal and description fragment to be compared in the behavioral level description and the RT level description which are specified by the correspondence information; and

means for determining, based on the comparison of the first logic cones and the second logic cones, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

23. (New) A logic verification method comprising the steps of:

inputting a behavioral level description written in a programming language, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair;

compiling the behavioral level description into an object code and compile information, wherein the object code is executable by the CPU, wherein the compile information includes mapping information which specifies information on a pair of a description fragment of the behavioral level description and a code portion of the object code and which specifies information on a pair of a signal in the behavioral level description and a variable in the object code;

searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

setting initial symbol values in the variables;

performing symbolic simulation from the start to end points of the code portion;

determining first logic cones of the variables as symbol values when the variable symbolic simulation ends;

extracting second logic cones each for the signals for each fragments of RT level description to be compared which are specified by the correspondence information;

selecting corresponding logic cones, as first selected logic cones, from among the logic cones determined in the determining step by referencing the compile information;

selecting corresponding logic cones, as second selected logic cones, from among the logic cones extracted in the extracting step by referencing the correspondence information;

comparing the first selected logic cones and the second selected logic cones, for each signal and description fragment to be compared in the behavioral level description specified by the correspondence information;

determining, based on the comparing step, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits; and

if the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first selected logic cones are logically equivalent to the second selected logic cones.

24. (New) A computer-readable medium embodying a computer program product and comprising code that, when executed, causes a computer to perform logic verification, the program product comprising the steps of:

a) storing a behavioral level description written in a programming language, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair;

b) compiling the behavioral level description into an object code and compile information, wherein the object code is executable by the CPU, wherein the compile information includes mapping information which specifies information on a pair of a description fragment of the behavioral level description and a code portion of the object code and which specifies information on a pair of a signal in the behavioral level description and a variable in the object code;

c) extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language;

d) extracting second logic cones from an RT level description;

e) selecting corresponding logic cones, as first selected logic cones, from among the logic cones determined in the step b) by referencing the compile information;

f) selecting corresponding logic cones, as second selected logic cones, from among the logic cones extracted in the step c) by referencing the correspondence information;

g) comparing the first selected logic cones and the second selected logic cones, for each signal and description fragment to be compared in the behavioral level description specified by the correspondence information; and

h) determining, based on the comparison of the first selected logic cones and the second selected logic cones, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable in a manufacturing phase for the logic circuits; and

i) if the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first selected logic cones are logically equivalent to the second selected logic cones,

wherein the step c) comprises the steps of:

c.1) searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

c.2) setting initial symbol values in the variables;

c.3) performing symbolic simulation from the start to end points of the code portion; and

c.4) determining the first logic cones of the variables as symbol values when the variable symbolic simulation ends.